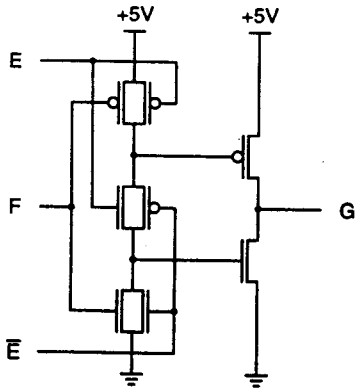
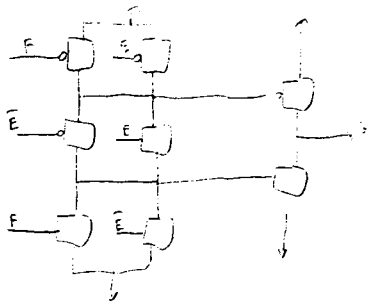
QUESTION #1

MARKS: 10 (10)

a) Determine the operation of the following circuit. A truth table is required.





E	F	G
0	0	Z
0	1	Z
1	0	0
1	1	1

10/

The middle two transistors form an enable (active high) controlled by input E, which causes the top and bottom sections together to form a single output to the inverter. When the top & bottom are not connected, E is LO which causes the top & bottom NOR is turned on so that G is in a high impedance state.

This is a tristate buffer with an active high enable

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a question."

QUESTION #2

MARKS: 15 (3 + 3 + 3 + 3 + 3)

Explain briefly, but as completely as possible, FIVE (5) of the following. A *SHORT* paragraph should be sufficient.

a) The diffusion layer is usually not used as a signal routing layer. Give THREE (3) reasons for this.

HIGH C } = SLOW
HIGH R }
ROUTING PROBLEMS (TRANSISTORS)
SPACE (# OF RULES)

b) The Metal 1 layer is usually used as the primary signal routing layer. Give THREE (3) reasons for this.

LOW C } = FAST
LOW R }
RUNS ANY WHERE
SIMPLE RULES

c) Where is the Canadian Microelectronics Corporation (CMC) located? Who does their fabrication? Why do they do their fabrication?

KINGSTON, ONTARIO (QUEEN'S UNIVERSITY)
GENNUM, MITEL, NORTEL (MOSIS)

HIRING POOL OF EDUCATED PEOPLE.
TAX BREAK

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d) Technically speaking, how many transmission gates does the circuit shown in Question #1 of this examination paper contain? Explain.

ONE

A T-GATE HAS A N-CHANNEL AND P-CHANNEL TRANSISTOR IN //. ONLY P_3 AND N_3 ARE CONNECTED LIKE THIS. MUST ALSO HAVE SIGNALS THAT ARE COMPLEMENTS (E AND $\bar{E}$).

e) Design rule D.1 indicates that the P-well to P+ Diff. Minimum Separation (see Appendix C: Available Process Technologies, page C9) is 14 design scale microns (dsm). Why is it so large? Using design rule D.1 as a start, what would the Minimum Separation design rule for P-well to P+ mask be if one existed? Why?

P+ DIFF WILL SHORT TO P-WELL! MUST ALSO ALLOW FOR ISOLATION (P-GUARDS, ETC.

10 D.S.M. (FROM RULE C.8)

ENCLOSURE RULE FOR P^+ MASK OVER DEVICE WELL

f) The CMOS fabrication process consists of a number of steps. Pick the ONE that you consider to be crucial to the success of fabrication. Discuss.

① INGOT MANUFACTURE
② MASKS (PREPARATION AND USE).
③ POLYSILICON DEPOSITION
ETC.

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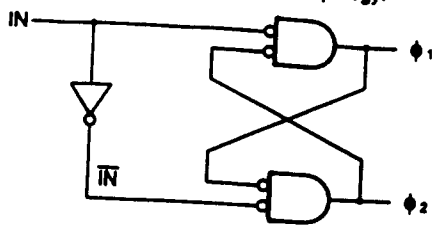
[Prof] "This question is one I fully expected you guys to bugger up."
[Student] "I didn't let you down, sir."

QUESTION #3

MARKS: 20 (20)

All parts of this question concern a two-phase (2φ) clock generator. The operation of the circuit is NOT important for this exam, just the topology.



$$\frac{\overline{A}\,\overline{B}}{A+B}$$

a) Draw a STICKS diagram for the two-phase circuit.

When doing your diagram the following constraints must be followed:

1. Input must come in from the left (on Metal 1).
2. Outputs must exit from the right (on Metal 1).
3. No wires are allowed outside the VDD and Vss Power rails.
4. At least two substrate connections (of each type) must be shown.
5. No Metal 2 is allowed.
6. Standard STICKS colors for the CMOS3DLM technology must be used.

Use the following page for your final two-phase STICKS diagram (indicate clearly which one it s). Your STICKS diagram will be marked using "good CMOS circuit design" guidelines as discussed n class.

"DEMORGAN"

CONTACT CUTS!! (MINIMUM # = 22)
SUBSTRATE CONNECTIONS
P+
P-WELL

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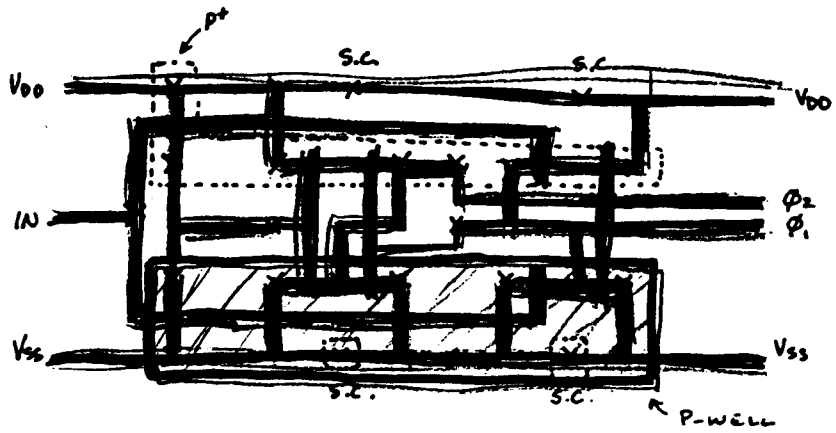
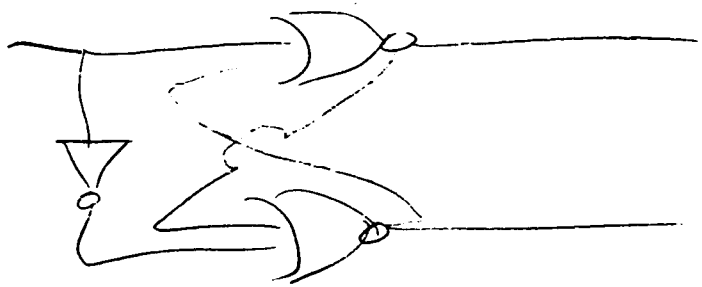
TWO-PHASE STICKS DIAGRAM



23 CONTACT CUTS (TOTAL)
2 S.C. TO VDD (FOR P-CHANNELS) OUTSIDE P+
2 S.C. TO VSS (FOR N-CHANNELS) INSIDE P+
INSIDE P-WELL



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"I try to set exams so you get no benefit from studying."